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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,542	03/17/2004	Mitsuaki Osame	740756-2717	2322

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,542	OSAME ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 9-30-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim1,4,7, 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US 6,670,773 B2).

As to claims 1,15 Nakamura et al. teaches a display device or a semiconductor device (col. 1, lines 11-17) comprising:

plural groups including a light emitting element and a thin film transistor which is connected to the light emitting element (fig. 2, items 11-13, col. 5,lines 50-57);

wherein an absolute value of a fluctuation rate of an ON current in a saturation region of a first thin film transistor included in a first group of said plural groups and a second thin film transistor included in a second group of said plural groups which is adjacent to the first group is not much experienced (col. 2, lines 37-43).

Nakamura does not disclose value of a fluctuation rate is at most 12%.

It would have been obvious to one of ordinary skill in the art at the time of invention that fluctuation rate which is not much experienced could be at most 12%, because actual rate will depend how much higher is gate potential than the threshold voltage of the transistor (col. 2, lines 37-41 in Nakamura et al. reference).

As to claim 4, Nakamura et al. teaches a display device (col. 1, lines 11-17) comprising:

plural groups including a thin film transistor and a light emitting element in which brightness is fluctuated depending on an ON current value in a saturation region of a drain voltage-drain current characteristic of the thin film transistor (fig. 2, items 11-13, col. 2, lines 37-43 and col. 5,lines 50-57);

wherein an absolute value of a fluctuation rate of an ON current in a saturation region of a first thin film transistor included in a first group of said plural groups and a second thin film transistor included in a second group of said plural groups which is adjacent to the first group is not much experienced (col. 2, lines 37-43).

Nakamura does not disclose value of a fluctuation rate is at most 12%.

It would have been obvious to one of ordinary skill in the art at the time of invention that fluctuation rate which is not much experienced could be at most 12%, because actual rate will depend how much higher is gate potential than the threshold voltage of the transistor (col. 2, lines 37-41 in Nakamura et al. reference).

As to claim 7, Nakamura et al. teaches a display device (col. 1, lines 11-17) comprising plural pixels including a driving thin film transistor (fig. 3,item 26), a switching thin film transistor (fig. 3,item 26), an erasing thin film transistor (fig. 3,items 12,24), a light emitting element which is connected to the driving thin film transistor (fig. 3,items 11,26, col. 7, lines 35-67);

wherein brightness is fluctuated depending on an ON current value in a saturation region of a drain voltage-drain current characteristic of the thin film transistor (fig. 2, items 11-13, col. 2, lines 37-43 and col. 5,lines 50-57);

an absolute value of a fluctuation rate of an ON current in a saturation region of a first thin film transistor included in each a first pixel and a second pixel which is adjacent to the first pixel is not much experienced (col. 2, lines 37-43).

Nakamura does not disclose value of a fluctuation rate is at most 12%.

It would have been obvious to one of ordinary skill in the art at the time of invention that fluctuation rate which is not much experienced could be at most 12%, because actual rate will depend how much higher is gate potential than the threshold voltage of the transistor (col. 2, lines 37-41 in Nakamura et al. reference).

As to claim 13, Nakamura et al. teaches a display device (col. 1, lines 11-17) comprising:

plural groups including a light emitting element and a thin film transistor which is connected to the light emitting element (fig. 2, items 11-13, col. 5,lines 50-57);

wherein an absolute value of a fluctuation rate of an ON current in a saturation region of a first thin film transistor included in a first group of said plural groups and a second thin film transistor included in a second group of said plural groups which is adjacent to the first group is not much experienced (col. 2, lines 37-43).

Nakamura does not disclose value of a fluctuation rate is at most 12% and a cellular phone comprising a main body, a display portion, a voice output portion, an operation switch, and an antenna.

It would have been obvious to one of ordinary skill in the art at the time of invention that fluctuation rate which is not much experienced could be at most 12%, because actual rate will depend how much higher is gate potential than the threshold

voltage of the transistor (col. 2, lines 37-41 in Nakamura et al. reference) and for use in a cellular phone comprising a main body, a display portion, a voice output portion, an operation switch, and an antenna (in reference : "for use in an image display apparatus_ (col. 1, lines 1-2).

As to claim 14, Nakamura et al. teaches a display device (col. 1, lines 11-17) comprising:

plural groups including a light emitting element and a thin film transistor which is connected to the light emitting element (fig. 2, items 11-13, col. 5,lines 50-57);

wherein an absolute value of a fluctuation rate of an ON current in a saturation region of a first thin film transistor included in a first group of said plural groups and a second thin film transistor included in a second group of said plural groups which is adjacent to the first group is not much experienced (col. 2, lines 37-43).

Nakamura does not disclose value of a fluctuation rate is at most 12% and a notebook computer comprising a main body, a case, a display portion, and a keyboard.

It would have been obvious to one of ordinary skill in the art at the time of invention that fluctuation rate which is not much experienced could be at most 12%, because actual rate will depend how much higher is gate potential than the threshold voltage of the transistor (col. 2, lines 37-41 in Nakamura et al. reference) and for use in notebook computer comprising a main body, a case, a display portion, and a keyboard (in reference : "for use in an image display apparatus" (col. 1, lines 1-2).

As to claims 10-12,16 Nakamura et al. teaches a display device (col. 1, lines 11-18).

3. Claims 2,5,8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. as applied to claims 2,4,7 above, and further in view of Sivan (US 5,229,310).

Nakamura et al. does not disclose the channel length of the first thin film transistor and the second thin film transistor is at least 5 times as long as a gate width, respectively.

Sivan teaches that channel length is determined by gate width which can vary considerably (col. 6, lines 45-47).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Sivan into Nakamura et al. system in order to provide channel length control (col. 2, lines 24-26 in Sivan refrence).

4. Claims 3,6,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. as applied to claims 2,4,7 above, and further in view of Gosain et al. (US 5,953,595).

Nakamura et al. does not disclose first thin film transistor and the second thin film transistor comprises a semiconductor layer which is formed by irradiating with a pulsed laser beam.

Gosain et al. teaches that channel length is determined by gate width which can vary considerably (fig. 8D, col. 11, lines 20-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teachings of Gosain et al. into Nakamura et al. system in order to manufacture TFT (col. 1, lines 5-8 in Gosain et al. reference).

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS

01.20.07

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